Barrier Coatings For Thin Film Solar Cells

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ABSTRACT

This paper describes studies of multiple layer barrier coatings for thin film solar cells. The main objective of the work is to develop low cost coatings for cells such as CIGSS that inhibit any significant moisture ingress and oxygen diffusion after 1000 hours of operation at 85/85 conditions. The general approach to coating application involves depositing alternate layers of polymer and inorganic films. The approach utilizes inorganic layers to provide barrier properties, while polymer layers planarize surface topography/defects, decouple defects/pinholes, and prevent damage in adjacent inorganic layers. Results are discussed for a coated and uncoated SSI CIGSS circuit. Initial results are very encouraging.

1. Introduction

A key issue facing thin film photovoltaic manufacturers is the need for an effective approach to module encapsulation. In particular, improved coatings are required to inhibit oxygen diffusion and moisture ingress. A second important concern particularly to the CdTe technology area is the need for improved understanding of degradation mechanisms operative in devices. The PNNL program which was initiated in September, 2002, is focused on these two important areas, namely: (1) Development of multilayer, barrier coatings for thin film cells; and (2) investigation of back contacts for CdTe cells, and their impact on cell stability.

This paper focuses on work carried out to date on barrier coatings. Investigations have involved studies with cells supplied by Shell Solar, Industries (SSI). CdTe back contact studies are being conducted in a collaborative effort with Dr. Sanpath's group at Colorado State University. These studies will be reported later.

2. Development Of Barrier Coatings At PNNL

Work has been conducted at PNNL to develop barrier coatings for organic light emitting diodes (OLEDs) since 1996. As illustrated in Fig. 1, the approach has involved combining a vacuum process for deposition of polymer films with the vacuum deposition of oxide layers to fabricate a multilayer barrier film structure. This approach is referred to as a Polymer Multi-Layer (or PML) process. These coatings can be deposited in a vacuum web coater or in a recently constructed in-line coater [1].

Coating requirements for OLEDs may be much more demanding than those appropriate to provide adequate life for solar cells. For example, it is estimated that for OLED devices to have reliable performance life times exceeding 10,000 hours, oxygen transmission rates (OTR) must be below 10^{-2} cc/m^2/d and water vapor transmission rates (WVTR) must between 10^{-6} and 10^{-5} g/m^2/d at 38 C and 95% RH. The barrier coating effort at PNNL has demonstrated WVTR values less than 2×10^{-7} g/m^2/d for coatings on glass [2].

These coatings are extremely effective in preventing oxygen and water penetration. This is a result of the inorganic layers providing the barrier properties, while the polymer layers planarize surface topography/defects, decouple defects/pinholes, and prevent damage (cracking) in adjacent inorganic layers. A tortuous path through the inorganic layers and polymer layers limits diffusion of gases and water vapor. Since physical vapor deposited layers replicate the surface topology of the substrate, high points in the underlying substrate cannot be smoothed by an inorganic layer. These features are also subject to mechanical damage during a coating process, which lead to defects in the deposited coating. Ideally, the initial polymer layer effectively planarizes defects and provides an ideal surface for inorganic film deposition.

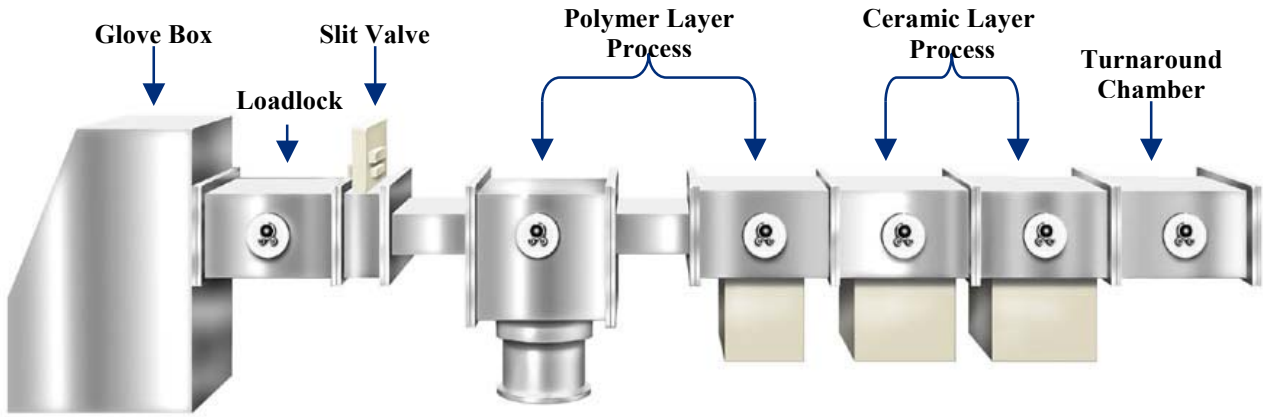

Figure 1. Schematic diagram of in-line coater to deposit multilayer barrier coatings.

3. Application To SSI CIGSS Circuits

A collaborative effort with SSI to develop barrier coatings for CIGSS modules has resulted in interesting and encouraging results. SSI is providing CIGSS monolithically integrated thin-film circuits which consist of ten cells connected in series on a 10 cm x 10 cm glass substrate. Each cell is approximately 0.69 cm x 8.3cm. A border region of approximately 0.8 cm is depleted by SSI for the purpose of these studies to allow a smooth coating at the edge of the circuit. The approach to applying multilayer coatings on the SSI circuits is illustrated in Fig. 2. Before coating the devices, the structures are cleaned since any debris on the surface may result in a pathway for water or oxygen diffusion after the coatings are applied. Since SSI is cutting the circuits out of larger modules, particles of glass constitute one type of debris. Shipping and handling the circuits can also lead to debris on the surface of these structures. These problems would not exist in a production process.

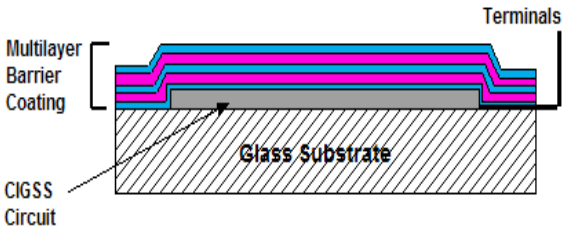

Figure 2. Schematic drawing of coated CIGSS circuit.

After cleaning circuits, they are then coated with a multilayer coating. Several variables are being considered in developing barrier layer coatings for the SSI cells. Initial emphasis is being placed on determining an approach to barrier coating deposition that will lead to acceptable lifetime performance for 1000 hours at 85 C and RH of 85%, regardless of the process complexity. Eventually, emphasis will be placed on optimizing the coating approach to provide for a low cost process. Testing at 85/85 conditions will be soon be established. However, to date, testing has been conducted at 60 C and 90 % RH.

I-V characteristics for an uncoated and a coated CIGSS circuit are compared in Figure 3. Between measurements, the SSI circuits were stored in a Tenney environmental nchamber at conditions of 60 C and 90% relative humidity. The coated circuit shows no degradation after 500 hours of testing. Illuminated characteristics were measuremed with an ELH bulb based simulator. A 2 cm x 2 cm CIGSS cell previously measured by NREL was used as a standard cell. The simulator is adjusted to give the same Jsc for the standard cell prior to testing the CIGSS circuits. Several other CIGSS circuits are under test. These results are preliminary, but are very encouraging. The SSI CIGSS surface is relatively rough, and thus it is expected that much is to be learned regarding requirements for optimum coating processes.

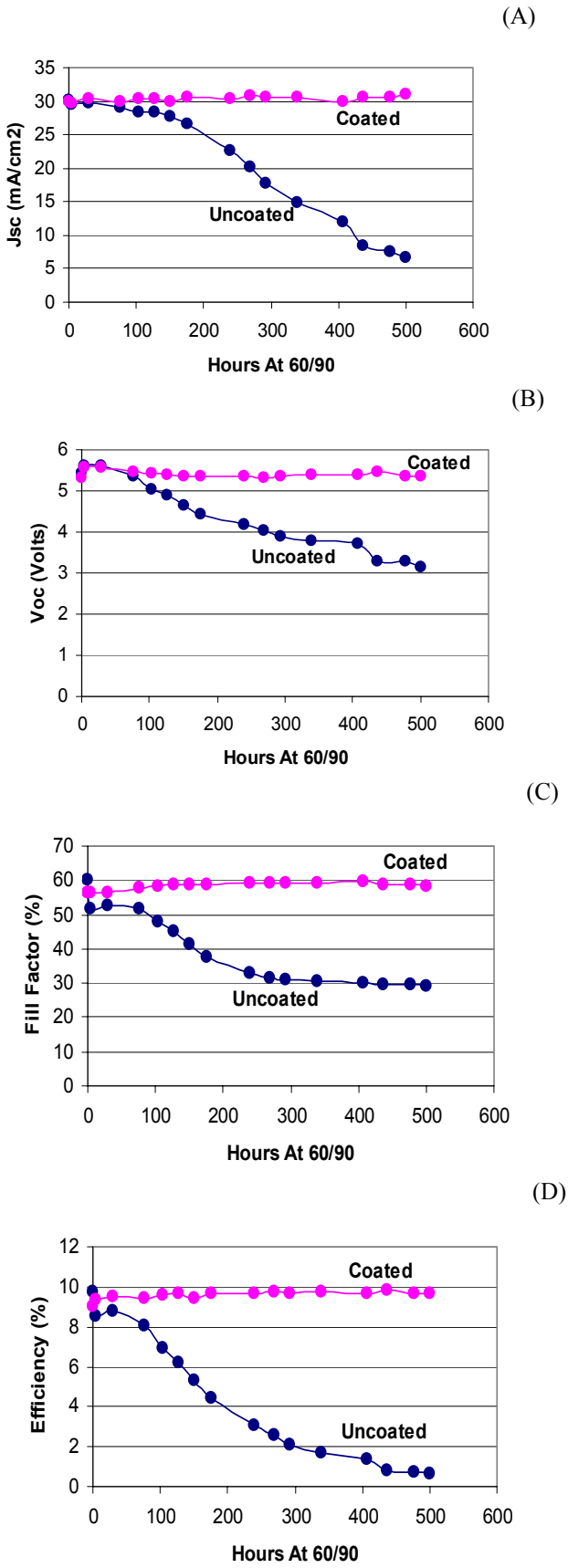

Figure 3. Comparison of Jsc, Voc, FF and efficiency for a coated and uncoated cell.

4. Other Work

Investigations of CdTe back contacts have begun. Initial efforts will concentrate on studies of back contacts based on Sb_2Te_3.

References

1. G. Graff, et. al, "Fabrication of OLED Devices on Engineered Plastic Substrates, "Proceedings of 2000 Society of Vacuum Coaters.
2. P. Martin, G. Graff and L. Olsen, "Barrier Coating Development at PNNL, Thin Film Module Reliability National Meeting, NREL, September 4-5, 2002.

Acknowledgements

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